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Design Automation Method for Total Ionization Dose Tolerant Integrated Circuits

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Abstract - **Modern integrated circuits (IC) operate in environment of various destabilizing factors which have essential influence on the operation of these circuits and often even disturb the normal operation. One of these destabilizing factors is the cosmic radiation, particularly total ionization dose effects (TID). For modern TID tolerant ICs [1-4] design is being done by circuit designers. In this paper an automation method is suggested which allows to replace transistors in layout with appropriate TID tolerant devices, where it is needed to have high tolerance from TID effects. This method allows design of TID tolerant IC layout by a design tool bringing to minimum circuit designer participation in layout design process.**

Keywords – **total ionization dose effects, design automation**

I. Introduction

It is known [1-4], that TID effects influence on threshold voltage, subthreshold and leakage currents, mobility of charge carriers (μ) and transconductance (g_m) of MOS transistors. Influence of TID effects on threshold voltages of MOS transistors are described in [1-2]. Threshold voltage should be measured as

$$V_{TH} = V_{TH0} + [\Delta V_{OT} + \Delta V_{IT}], \qquad (1)$$

where V_{TH0} is pre-irradiation threshold voltage, ΔV_{OT} is the change in threshold voltage due to holes trapped at the interface and ΔV_{IT} is the change caused by the charging of interface traps. For n-MOS transistor ΔV_{OT} decreases the threshold voltage [1-2]. For p-MOS transistor ΔV_{OT} increases the magnitude of threshold voltage. For both n-MOS and p-MOS ΔV_{IT} should be taken positive. Finally ΔV_{OT} and ΔV_{IT} should be measured as [2]

$$\Delta V_{OT} = -3.8 \cdot 10^{-8} \cdot t_{OX}^2 \cdot D \qquad (2)$$

$$\Delta V_{IT} = 2.4 \cdot 10^{-8} \cdot t_{OX}^2 \cdot D^{2/3}, \qquad (3)$$

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where D is the radiation dose in rads, tox is the gate oxide thickness in nanometers.

Description about subthreshold and leakage currents can be found in [3]. Subthreshold current of a n-MOS transistor can be measured by the following equation:

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot \exp \frac{V_{GS} - V_{THN}}{V_T}, \qquad (4)$$

where I_D is the drain current of transistor, W/L are the sizes of transistor, VGS is the gate-source voltage of transistor, $V_T = KT/q$ is the thermal voltage and V_{THN} is threshold voltage. Subthreshold current can change due to two factors. One of them is the threshold voltage change due to TID effects influence. The second reason is shown in figure 1. Except the main channel, two parasitic channels are being farmed in MOS fabrication process (figure 1) [4]. Due to TID effects influence of these parasitic transistors becomes notable. As a result, subthreshold current changes.

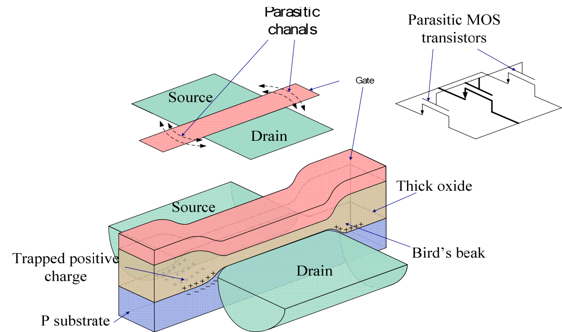


Figure 1. Parasitic transistors' influence increase due to TID effects

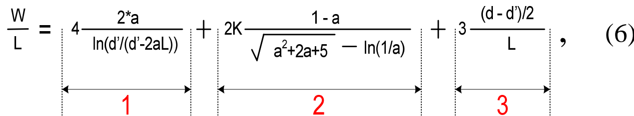
Description of mobility changes of charge carriers and transistor transconductance changes due to TID effects influence is given in [3]. Mobility of charge carriers is being measured as

$$\mu = \frac{\mu_0}{1 + \alpha * (\Delta N_{it})}, \qquad (5)$$

where μ_0 is the pre-irradiation mobility, ΔN_{it} is the number of interface traps per unit area introduced by ionizing radiation. α is a technology dependant parameter ($\alpha = 7 \pm 1.3 \times 10^{-13}$). Dependences of mobility from radiation dose for both electron and hole are presented in figure 2.

There are several methods [4] which are used to protect MOS transistors from TID effects. The most effective method, which provides the highest level of protection from TID effects, is given in [4] and is called enclosed layout topology (ELT). Transistor with ELT

structure is presented in figure 3. The main disadvantages of ELT transistor are that it is difficult to measure the W/L ratio of MOS transistor and area of this transistor is more than area of classical MOS device. To calculate W/L ratio of this kind of MOS transistor, it is being introduced as three transistors, connected in parallel (figure 3). W/L ratio of ELT transistor is being measured as



$$\frac{W}{L} = \underbrace{4\frac{2^{*}a}{\ln(d'/(d'-2aL))}}_{1} + \underbrace{2K\frac{1-a}{\sqrt{a^2+2a+5}-\ln(1/a)}}_{2} + \underbrace{3\frac{(d-d')/2}{L}}_{3}, \quad (6)$$

where K is a geometry dependent parameter (if L<=0,5um, then K=3,5, else if L>0,5um, K=4), a is a connecting parameter between transistors 1 and 2 (figure 3).

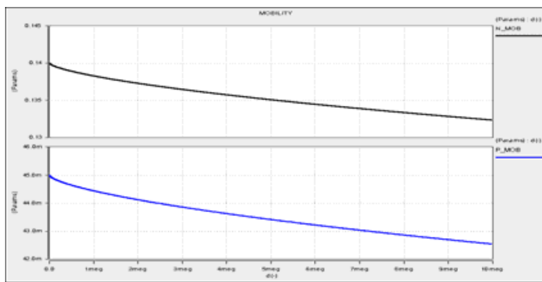


Figure 2. Dependences of mobility from radiation dose

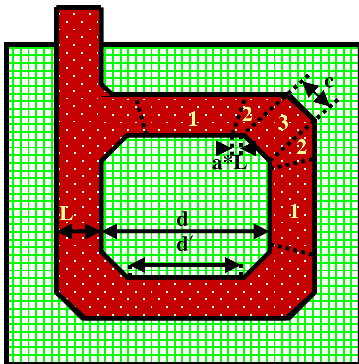


Figure 3. ELT transistor structure

Equation (6) shows that it is rather difficult to calculate W/L ratio for ELT transistor. For TID hardening of circuits with large number of devices it will be rather difficult to calculate W/L ratios for all transistors to replace them with ELT devices. A design automation method is proposed in this paper, which allows to replace all the transistors in parts of the circuits, which need to be TID hardened, by ELT transistors automatically. In this case W/L ratio is being calculated automatically, too. This calculation is based on equation (6). Operation of the provided design tool is schematically presented in figure 4. Layout of a simple inverter is presented. Lets assume that the n-MOS transistor needs to be TID tolerant (figure 4). One just needs to input to suggested program the name of the device, which must be replaced. The program will calculate the sizes of ELT transistor appropriate to W/L ratio of the transistor from original design. After replacement tool does the routing as well. For routing pin/port names should be kept the same, as in original design.

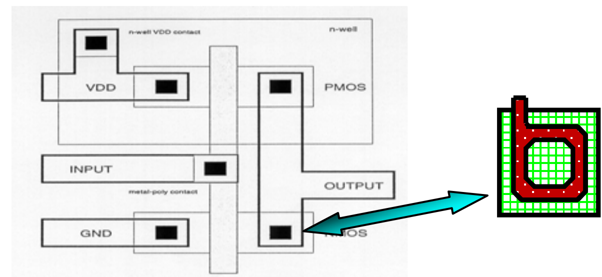


Figure 4. Operation principle of the suggested tool

Transistor characteristics before and after irradiation are shown in figure 5 [3]. It can be seen, that for 0.25um technology pre- and post-irradiation curves are almost the same (with the use of ELT transistor).

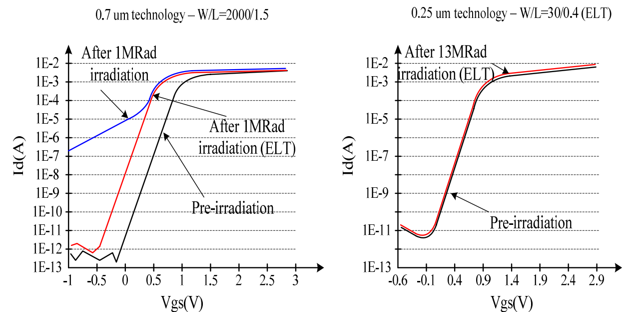


Figure 5. Transistor I/V characteristics before and after irradiation

II. Conclusion

Thus, presented method provides TID tolerant design automation. It helps to reduce job connected with human factor. It means mistake probability is less too. Design time is being reduced as well, because the W/L ratio calculations are being done automatically. But this method has disadvantages too: it uses only one of the known methods of TID hardening of ICs. ELT transistor method, which is used in design automation tool, provides the best protection from TID, but sizes of IC are being increased. Provided method can be used in cases when chip area is not critical, but high TID tolerance is needed.

References

[1]. D. Pan, H. W. Li, B. W. Milamowski A Radiation-Hard Phase-Locked Loop // Industrial Electronics, ISIE '03, IEEE International Symposium. -June 9-11, 2003. -Vol. 2. -P.901-906.

[2]. J. R. Srour, J. M. McGarrity Radiation Effects on Microelectronics in Space // Proceedings of the IEEE. -November, 1988. -Vol. 76, No. 11. -P.1443-1469

[3]. A. P. Gnana Prakash, S. C. Ke, K. Siddappa High-energy radiation effects on subthreshold characteristics, transconductance and mobility of n-channel MOSFETs // Semiconductor Science and Technology. -2003. -Volume 18, No. 12. -P.1037-1042.

[4]. A. Stabile, V. Liberali, C. Calligaro Design of a rad-hard library of digital cells for space applications // 15th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2008. -Aug. 31 2008-Sept. 3 2008. -P.149-152.